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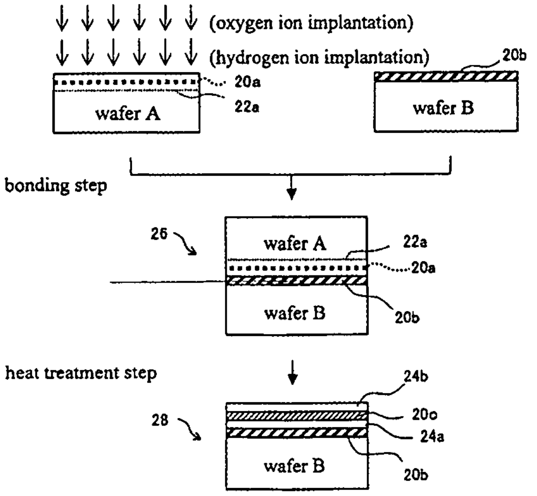
(54) SEMICONDUCTOR WAFER AND METHOD FOR PRODUCING THE SAME

(57) There is provided a novel bonded semiconductor wafer having a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more and manufactured by means of a bonding process, wherein at least one of the insulator layers is formed with ion implanted oxygen, and a novel manufacturing process for a bonded semiconductor wafer in which an ion implantation separation process is adopted. The novel bonded semiconductor wafer is manufactured by means of a bonding process and has a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more, wherein at least one of the insulator layers is formed with ion implanted oxygen.

FIG. 1



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Description

Technical Field

[0001] The present invention relates to a bonded semiconductor wafer having a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more and to a novel manufacturing process therefor.

Background Art

[0002] In the technical progress in miniaturization of LSI (Large Scale Integrated circuit) devices in recent years, more perfect isolation, a higher operating speed and higher performance have been pursued and attention has been given to an SOI (Silicon-On-Insulator) wafer as material satisfying such demands.

[0003] There has been known a wafer bonding process as one of the manufacturing techniques for an SOI wafer. As a technique utilizing this bonding process, a so-called ion implantation separation process (also called a Smart-Cut (a registered trade mark) process) has been developed, which is described in JP A 93-211128.

[0004] This ion implantation separation process is a technique wherein an oxide film is formed on at least one of two silicon wafers, hydrogen gas ions or rare gas ions are implanted into one silicon wafer through an upper surface thereof to form a micro-bubble layer (an enclosed layer) within the interior of the one silicon wafer, thereafter the ion implanted surface is put into close contact with the other wafer with the oxide film interposed therebetween, then heat treatment (separation heat treatment) is applied to the wafers in close contact to separate the one wafer in such a manner that the contact portion is partly left in a state of a thin film at the micro-bubble layer performing as a cleavage plane (a separation plane), and heat treatment (bonding heat treatment) is further applied to the other wafer with the thin film left thereon to reinforce bonding between the surfaces in close contact and thereby manufacture an SOI wafer.

[0005] In this process, an SOI wafer is obtained with relative ease in which the separated surface is a good mirror surface and the SOI layer is very high in uniformity. This process is also advantageous in that a raw material can be effectively used since one wafer partly removed by separation can be reused. Furthermore, this process makes it possible that two silicon wafers can be bonded directly with each other without an oxide film interposed therebetween, not limited to the case where two silicon wafers are bonded together, the ion implanted silicon wafer is bonded to an insulator wafer having a different thermal expansion coefficient such as of quartz, silicon carbide and alumina, or by selecting a material other than silicon as a wafer to be ion implanted, a bonded wafer having a thin film of the material can be manufactured.

[0006] With the advent of the ion implantation separation process, there is solved a problem of film thickness uniformity which is the greatest problem in a bonded semiconductor wafer, and it has been possible to manufacture a bonded SOI wafer with a film thickness uniformity as excellent as 1 nm or less in film thickness standard deviation across a surface of the SOI layer. This process has made possible application of a bonded SOI wafer to an LSI such as a CMOS as a leading device, which requires an SOI layer in the form of an ultra-thin film and excellent film thickness uniformity, in addition to its conventional applications to a BiCMOS and a power IC.

[0007] While an SOI wafer to be used in the above-mentioned applications is of a structure including a single SOI layer formed on a buried oxide film, the applicant of the present application has proposed a technique in a previous application (JP A 99-316154) that the ion implantation separation process is adopted to form a bonded semiconductor wafer alternately stacked with two kinds of layers having different refractive indexes such as a combination of an SOI layer and a buried oxide film in two cycles or more and the bonded silicon wafer is utilized in an optical functional device.

[0008] This technique is to cultivate a field where the bonded semiconductor wafer is utilized in an optical functional device such as a waveguide, an optical communication modulator, an optical detector or a laser, and very useful. Especially, an SOI wafer having the simplest two cycle layered structure in such layered structures makes advantageously possible that an upper SOI layer is utilized in fabrication of an LSI while an lower SOI layer is utilized as an optical waveguide or a wiring layer, thereby facilitating three-dimensional wiring.

[0009] Description will be given of examples of prior art steps for manufacturing a bonded semiconductor wafer having a two cycle layered structure by use of the ion implantation separation process on the basis of FIGs. 4 and 5. FIG. 4 is a flow chart showing an example of a prior art manufacturing process for a bonded semiconductor wafer. FIG. 5 is a flow chart showing another example of a prior art manufacturing process for a bonded semiconductor wafer.

[0010] In FIG. 4, first of all, there are prepared a semiconductor wafer A having an insulator film or an insulator layer 10a on a surface thereof and a semiconductor wafer B having no insulator film on a surface thereof. Hydrogen (or rare gas) ions are implanted into the wafer A to form a micro-bubble layer 12a in the interior of the wafer A. The wafer A with the micro-bubble layer 12a is bonded to the wafer B with the insulator film 10a interposed therebetween at room temperature to form a bonded wafer 15.

[0011] When the bonded wafer 15 is heat treated, cracking occurs in the wafer A at the micro-bubble layer 12a due to strain to form an SOI wafer 16 with a one cycle layered structure in which the insulator layer 10a and a semiconductor layer 14a are formed on the wafer B. As opposed to the SOI wafer 16 with a one cycle layered structure, there is further prepared a wafer C having an insulator film or an insulator layer 10b on a surface thereof, hydrogen (or rare gas) ions are implanted into the wafer C to form a micro-bubble layer 12b in the interior of the wafer C. The wafer C with the micro-bubble layer 12b is bonded to the SOI wafer 16 at room temperature to form a bonded wafer 17.

[0012] When the bonded wafer 17 is heat treated, cracking occurs in the wafer C at the micro-bubble layer 12b to form an SOI wafer 18 with a two cycle layered structure in which the insulator layer 10b and the semiconductor layer 14b constituting the second cycle layered structure are formed on the first cycle layered structure (the insulator layer 10a and the semiconductor layer 14a) of the SOI wafer 16.

[0013] In another example of a prior art process shown in FIG. 5, a manufacturing process goes according to the same steps as in FIG. 4 till the first cycle layered structure is formed on a wafer B and as opposed to the SOI wafer 16 there is further prepared a wafer C having an insulator film or an insulator layer 10b on a surface thereof. In this prior art example, hydrogen (or rare gas) ions are implanted into the SOI wafer 16 to form a micro-bubble layer 12c in the interior of the SOI wafer 16 instead of ion implantation on the wafer C in FIG. 4.

[0014] Then, the SOI wafer 16 is bonded to the wafer C with the insulator film 10b interposed therebetween at room temperature to form a bonded wafer 17. When the bonded wafer 17 is heat treated, cracking occurs in the wafer C due to strain at the micro-bubble layer 12c, and the insulator layer 10b and a semiconductor layer 14c are further formed in addition to the one cycle layered structure (the insulator layer 10a and the semiconductor layer 14a) of the SOI wafer 16 to complete an SOI wafer 18 having a two cycle layered structure.

[0015] As described above, in any of the manufacturing processes of FIGs. 4 and 5, there are necessarily repeated two times the hydrogen (or rare gas) ion implantation step and the bonding step, respectively. Furthermore, at least two heat treatment steps are required for separation heat treatment, and when separation heat treatment and bonding heat treatment are separately performed, further heat treatment steps are added.

[0016] In manufacturing the bonded semiconductor wafer having such a layered structure, however, there has to be repeated the bonding step requiring the severest process control for the purpose to improve the manufacture yield, so the manufacturing processes are neither simple nor convenient, resulting in high frequency in occurrence of defective products in the bonding steps.

Disclosure of the Invention

[0017] The inventors have conducted earnest studies on a manufacturing process capable of manufacturing a bonded semiconductor wafer having a cyclically layered structure including semiconductor layers and insulator layers, and especially, a two cycle layered structure which is the simplest and most valuable in utilization among such cyclically layered structures, with more ease and further reduced frequency in occurrence of defective products, and as a result, have reached a conception that the number of bonding steps can be reduced by utilizing an oxide layer generated by oxygen ion implantation as an insulator layer, and completed the present invention on the basis of the conception.

[0018] With the above described problems in view, it is an object of the present invention to provide a novel bonded semiconductor wafer having a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more and manufactured by means of a bonding process, wherein at least one of the insulator layers is formed with ion implanted oxygen, and a novel manufacturing process for a bonded semiconductor wafer in which an ion implantation separation process is adopted, and capable of simplifying a manufacturing procedure and reducing defective products in the bonding steps.

[0019] In order to solve the above described problem, a bonded semiconductor wafer of the present invention is manufactured by means of a bonding process and has a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more, wherein at least one of the insulator layers is formed with ion implanted oxygen.

[0020] It is preferable that the semiconductor layers are of silicon and the insulator layers are of silicon oxide films, and the number of cycles of the layered structure is 2.

[0021] A first aspect of a manufacturing process for a bonded semiconductor wafer of the present invention comprises the steps of: preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed; implanting oxygen ions and hydrogen or rare gas ions into one surface of the first semiconductor wafer; thereafter bonding the surface of the first semiconductor wafer into which the ions have been implanted and a surface of the second semiconductor wafer with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; heat treating the bonded semiconductor wafer, thereby the first semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

[0022] In the first aspect, while an implantation depth of hydrogen ions or rare gas ions is required to be deeper than that of oxygen ions, there is no specific limitation as to which of both of the ion implantation steps is to be first performed.

[0023] A second aspect of a manufacturing process for a bonded semiconductor wafer of the present invention comprises the steps of : preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed; implanting oxygen ions into one surface of the first semiconductor wafer; implanting hydrogen ions or rare gas ions into one surface of the second semiconductor wafer; bonding the surface of the first semiconductor wafer and the surface of the second semiconductor wafer into each of which the ions have been implanted with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; and heat treating the bonded semiconductor wafer, thereby the second semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

[0024] A third aspect of a manufacturing process for a bonded semiconductor wafer of the present invention comprises the steps of: preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed; implanting oxygen ions into one surface of the first semiconductor wafer; thereafter heat treating the first semiconductor wafer to make an oxygen ion implanted layer of good film quality; further implanting hydrogen ions or rare gas ions into the one surface of the first semiconductor wafer; thereafter bonding the one surface of the first semiconductor wafer into which the ions have been implanted and a surface of the second semiconductor wafer with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; and heat treating the bonded semiconductor wafer, thereby the first semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

[0025] While the third aspect is a modification of the first aspect, wherein an SOI wafer is once manufactured by means of a so-called SIMOX (Separation by IMplanted OXygen) method and thereafter hydrogen ions are implanted on the SOI wafer, the subsequent steps being performed.

Brief Description of the Drawings

[0026]

FIG. 1 is a flow chart showing a first embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention;

FIG. 2 is a flow chart showing a second embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention;

FIG. 3 is a flow chart showing a third embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention;

FIG. 4 is a flow chart showing an example of a prior art manufacturing process for a bonded semiconductor wafer; and

FIG. 5 is a flow chart showing another example of a prior art manufacturing process for a bonded semiconductor wafer.

Best Mode for Carrying out the Invention

[0027] Description will be given of embodiments of the present invention taking up an SOI wafer having a two cycle layered structure as an example below on the basis of FIGs. 1 to 3 among the accompanying drawings. It is needless to say that various modifications or alterations of the embodiments can be carried out as far as not departing from the technical concept of the present invention. FIG. 1 is a flow chart showing a first embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention. FIG. 2 is a flow chart showing a second embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention. FIG. 3 is a flow chart showing a third embodiment of a manufacturing process for a bonded semiconductor wafer of the present invention.

[0028] In the first embodiment of the present invention shown in FIG. 1, first of all, a first semiconductor wafer A (for example, a silicon wafer) having no insulator film and a second semiconductor wafer B (for example, a silicon wafer) having an insulator film or an insulator layer (for example, an oxide film) 20b are prepared. Two kinds of ions, oxygen ions and hydrogen ions (or rare gas ions), are implanted into the wafer A. By these ion implantation steps, an oxygen ion implanted layer 20a and a hydrogen ion implanted layer (a micro-bubble layer) 22a are formed in the interior of the wafer A. In this case, while an implantation depth of hydrogen ions (or rare gas ions) is required to be deeper than that of oxygen ions, there is no specific limitation as to which of both of the ion implantation steps is to be first performed.

[0029] Then, the ion implanted wafer A is bonded to the wafer B with the insulator layer 20b interposed therebetween to form a bonded wafer 26. This bonding step is to be performed in a clean atmosphere at room temperature. After that, the bonded wafer 26 is heat treated. By this heat treatment, the oxygen implanted layer 20a is changed to an oxide film layer, that is, an insulator layer 20c, and a portion of the wafer A is separated from the bonded wafer 26 at the hydrogen ion implanted layer (a micro-bubble layer) 22a. By this separation, there is manufactured a bonded semiconductor wafer having a two cycle layered structure (the insulator layer 20b, a semiconductor layer 24a, the insulator layer 20c and a semiconductor layer 24b), that is, an SOI wafer 28 having the two cycle layered structure.

[0030] When the bonded wafer 26 is heat treated, low temperature heat treatment at temperature on the order of 400 to 600°C is sufficient if the heat treatment is performed only for the purpose of separation of the first wafer A, but in order to make the oxygen ion implanted layer 20a and the SOI layer adjacent thereto good in quality, heat treatment at temperature of 1300°C or higher is usually required. Therefore, the film quality improving heat treatment and the separation heat treatment can be concurrently performed in high temperature heat treatment, omitting the low temperature separation heat treatment. In the embodiment of FIG. 1, there is shown the case where the oxygen ion implanted layer 20a is changed to an oxide film layer (an insulator layer) 20c.

[0031] According to the first embodiment shown in FIG. 1, compared with the prior art processes shown in FIGs. 4 and 5, only one bonding step is required and the number of heat treatment steps can also be reduced; therefore, a manufacturing process becomes simpler and more convenient and defective products in the bonding step can be reduced.

[0032] In the second embodiment of the present invention shown in FIG. 2, similar to the case of FIG. 1, first of all, a first semiconductor wafer A (for example, a silicon wafer) having no insulator film and a second semiconductor wafer B (for example, a silicon wafer) having an insulator film or an insulator layer (for example, an oxide film) 20b are prepared. Oxygen ions are implanted into the wafer A to form an oxygen implanted layer 20a in the interior thereof. Hydrogen ions (or rare gas ions) are implanted into the wafer B to form an hydrogen ion implanted layer (a micro-bubble layer) 22a in the interior thereof.

[0033] Then, the wafer A implanted with oxygen ions is bonded to the wafer B implanted with hydrogen ions with the insulator film 20b interposed therebetween to form a bonded wafer 26. Following to this, the bonded wafer 26 is heat treated. By this heat treatment, the oxygen ion implanted layer 20a is changed to an oxide layer, that is, an insulator layer 20c, and a portion of the wafer B is also separated from the bonded wafer 26 at the hydrogen ion implanted layer (the micro-bubble layer) 22b. By this separation, there is manufactured a bonded semiconductor wafer having a two cycle layered structure (the insulator layer 20c, a semiconductor layer 24a, the insulator layer 20b and a semiconductor layer 24b), that is, an SOI wafer 28 having the two cycle layered structure.

[0034] According to the second embodiment shown in FIG. 2 as well, only one bonding step is required and the number of heat treatment steps can also be reduced; therefore, a manufacturing process becomes simpler and more convenient and defective products in the bonding step can be reduced.

[0035] The third embodiment of the present invention shown in FIG. 3 is a modification of FIG. 1, and similar to the case of FIG. 1, first of all, a first semiconductor wafer A (for example, a silicon wafer) having no insulator film and a second semiconductor wafer B (for example, a silicon wafer) having an insulator film or an insulator layer (for example, an oxide film) 20b are prepared. Oxygen ions are implanted into the wafer A to form an oxygen ion implanted layer 20a in the interior thereof, and thereafter high temperature heat treatment is applied thereto to form an SOI wafer 25 having a one cycle layered structure (an insulator layer 20c and a semiconductor layer 24a). That is, an SOI wafer according to the so-called SIMOX (Separation by IMplanted OXygen) method is once manufactured and thereafter, hydrogen ions are implanted on the SOI wafer, followed by the below described steps.

[0036] Hydrogen ions (or rare gas ions) are implanted into the SOI wafer 25 in which the one cycle layered structure is formed to form a hydrogen ion implanted layer (a micro-bubble layer) 22c in the interior thereof. Then, the SOI wafer 25 thus implanted with hydrogen ions is bonded to the wafer B with an insulator film 20b interposed therebetween to form a bonded wafer 26.

[0037] Then, the bonded wafer 26 is heat treated and thereby, a portion of the wafer A is separated from the bonded wafer 26 at a hydrogen ion implanted layer (a micro-bubble layer) 22c. By this separation, there is provided a bonded semiconductor wafer having a two cycle layered structure (the insulator layer 20b, a semiconductor layer 24a, the insulator layer 20c and a semiconductor layer 24b), that is, an SOI wafer 28 having the two cycle layered structure.

[0038] In the third embodiment of the present invention shown in FIG. 3, only one bonding step is required; therefore, a manufacturing process becomes simpler and more convenient and defective products in the bonding step can also be reduced.

[0039] Note that while in each of FIGs. 1 to 3, the insulator film or the insulator layer (for example, an oxide film) 20b prior to the bonding is formed on the wafer B, the insulator film 20b may be formed on either surface or both surfaces of the A and B wafers.

[0040] Furthermore, a layered structure of 3 cycles or more can be obtained by the following procedures; for example, a hydrogen ion implanted wafer (a wafer similar to the wafer B of FIG. 2) separately prepared is bonded to the surface of the SOI wafer 28 having a two cycle layered structure obtained according to any of the manufacturing processes of FIGs.1 to 3 and then separation heat treatment step is successively performed, or SOI wafers having multi-cycle layered structure are bonded together at respective surfaces thereof with the insulator film interposed therebetween.

Examples

[0041] Description will be given of the present invention taking up examples and needless to say that the examples should not be construed by way of limitation.

(Example 1)

[0042] Two silicon wafers of 200 mm in diameter and a <100> orientation were prepared. A bonded semiconductor wafer having a two cycle layered structure was manufactured according to the flow chart shown in FIG. 2 and under manufacturing conditions shown in Table 1. Results of the manufacture are shown in Table 1 as well. As shown in the results of the manufacture of Table 1, there was manufactured a bonded semiconductor wafer having a two cycle layered structure of good performance.

Table 1

	Wafer A	Wafer B
Surface oxide film	none	100 nm
Implanted ion	oxygen ion (O^+)	hydrogen ion (H^+)
Implantation energy	180keV	35keV
Dose	$4 \times 10^{17}/cm^2$	$8 \times 10^{16}/cm^2$
Heat treatment	1350°C, 4 hours	
Manufactured two cycle layered structure	surface SOI layer: 200 nm upper oxide film: 100 nm interior SOI layer: 300 nm lower oxide film: 80 nm (oxygen ion implanted oxide film)	

[0043] Furthermore, other bonded semiconductor wafers each having a two cycle layered structure were likewise manufactured according to the flow charts shown in FIGs. 1 and 3, and bonded semiconductor wafers each having good performance were obtained.

Capability of Exploitation in Industry

[0044] According to the present invention, as described above, there can be provided a novel bonded semiconductor wafer having a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more, and manufactured by means of a bonding process, wherein at least one of insulator layers is formed with ion implanted oxygen. Further, according to a manufacturing process of a bonded semiconductor wafer of the present invention, an ion implantation separation process is adopted, thereby enabling simplification of a manufacturing procedure and reduction of defective products in a bonding step.

Claims

1. A bonded semiconductor wafer manufactured by means of a bonding process and having a layered structure alternately stacked with semiconductor layers and insulator layers in two cycles or more, wherein at least one of the insulator layers is formed with ion implanted oxygen.

2. The bonded semiconductor wafer according to claim 1, wherein the semiconductor layers are of silicon and the insulator layers are of silicon oxide films, and the number of cycles of the layered structure is 2.

3. A manufacturing process for a bonded semiconductor wafer, comprising the steps of:

   preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed;
   implanting oxygen ions and hydrogen or rare gas ions into one surface of the first semiconductor wafer;
   thereafter bonding the surface of the first semiconductor wafer into which the ions have been implanted and a surface of the second semiconductor wafer with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; and
   heat treating the bonded semiconductor wafer, thereby the first semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

4. A manufacturing process for a bonded semiconductor wafer, comprising the steps of:

preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed;
implanting oxygen ions into one surface of the first semiconductor wafer;
implanting hydrogen ions or rare gas ions into one surface of the second semiconductor wafer;
bonding the surface of the first semiconductor wafer and the surface of the second semiconductor wafer into each of which the ions have been implanted with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; and
heat treating the bonded semiconductor wafer, thereby the second semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

5. A manufacturing process for a bonded semiconductor wafer, comprising the steps of:

preparing first and second semiconductor wafers on one or both of which an insulator film or insulator films are formed;
implanting oxygen ions into one surface of the first semiconductor wafer;
thereafter heat treating the first semiconductor wafer to make an oxygen ion implanted layer of good film quality:

> further implanting hydrogen ions or rare gas ions into the surface of the first semiconductor wafer;
> thereafter bonding the surface of the first semiconductor wafer into which the ions have been implanted and a surface of the second semiconductor wafer with the insulator film or films interposed therebetween to form a bonded semiconductor wafer; and
> heat treating the bonded semiconductor wafer, thereby the first semiconductor wafer being separated from the bonded semiconductor wafer at a micro-bubble layer formed by the implantation of hydrogen ions or rare gas ions.

FIG. 1

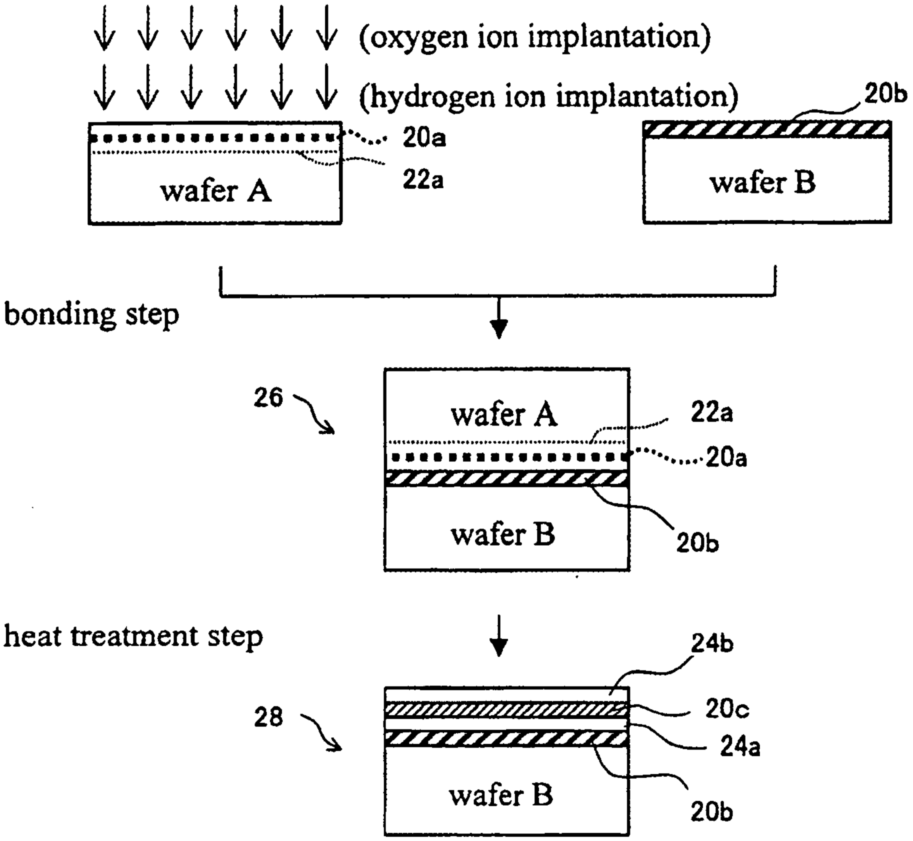

(oxygen ion implantation)
(hydrogen ion implantation)
20b
20a
22a
wafer A
wafer B
bonding step
26
wafer A
22a
20a
wafer B
20b
heat treatment step
24b
28
20c
24a
wafer B
20b

FIG. 2

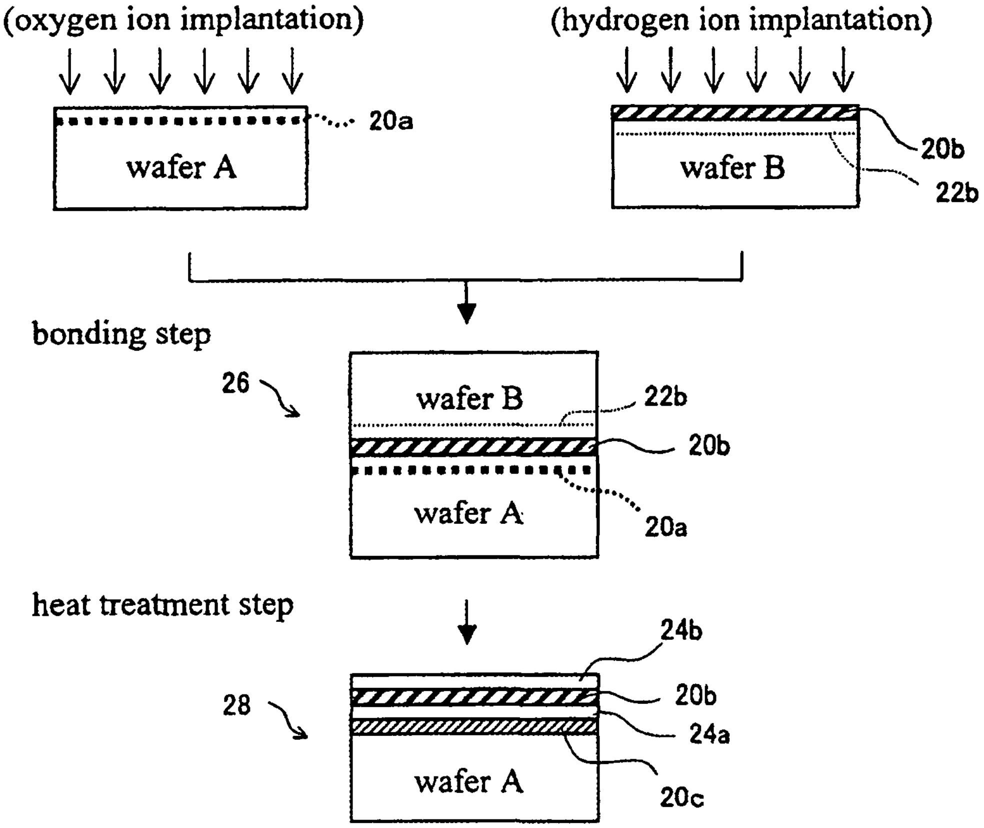

(oxygen ion implantation)
(hydrogen ion implantation)
20a
wafer A
wafer B
20b
22b
bonding step
26
wafer B
22b
20b
wafer A
20a
heat treatment step
24b
28
20b
24a
wafer A
20c

FIG. 3

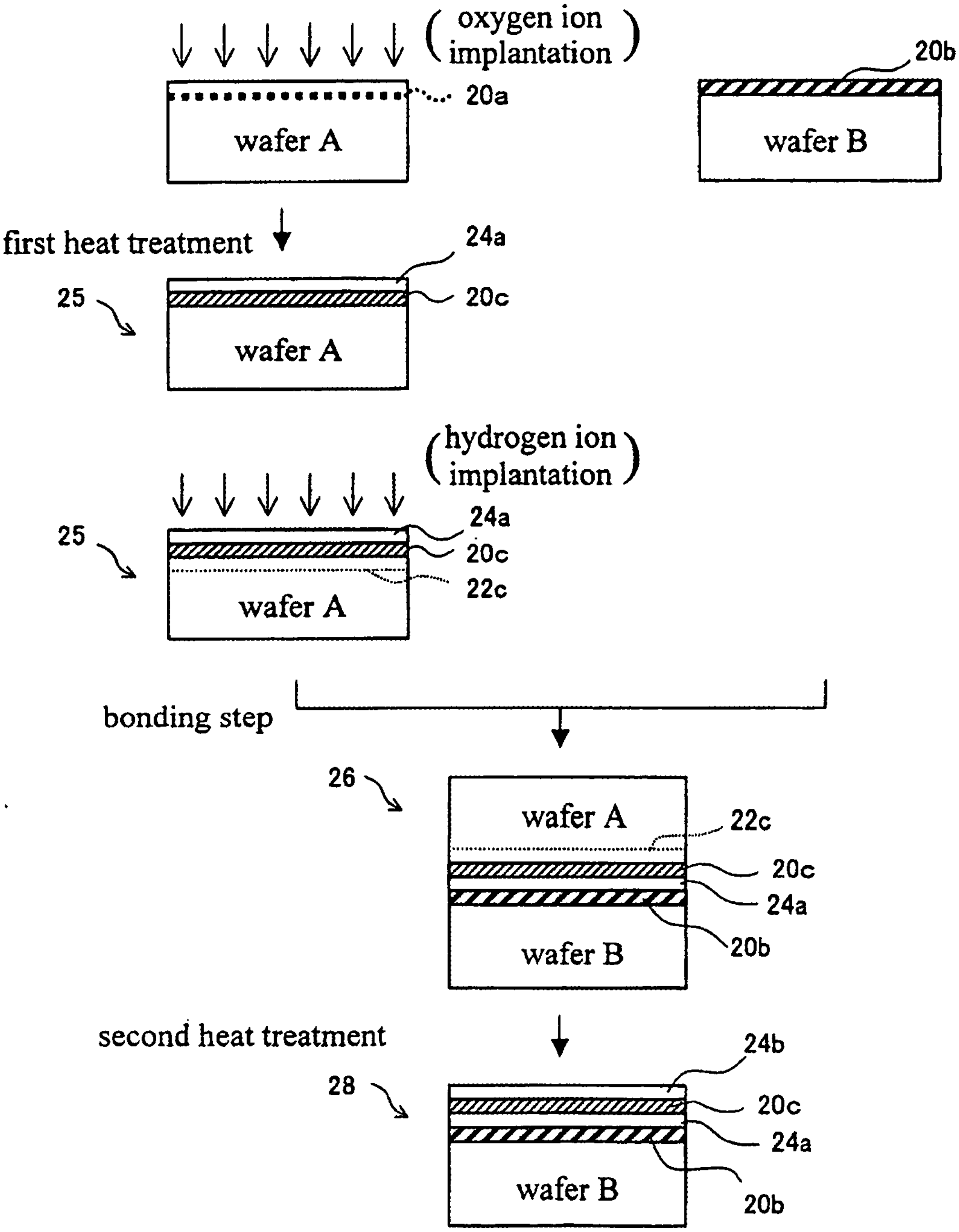
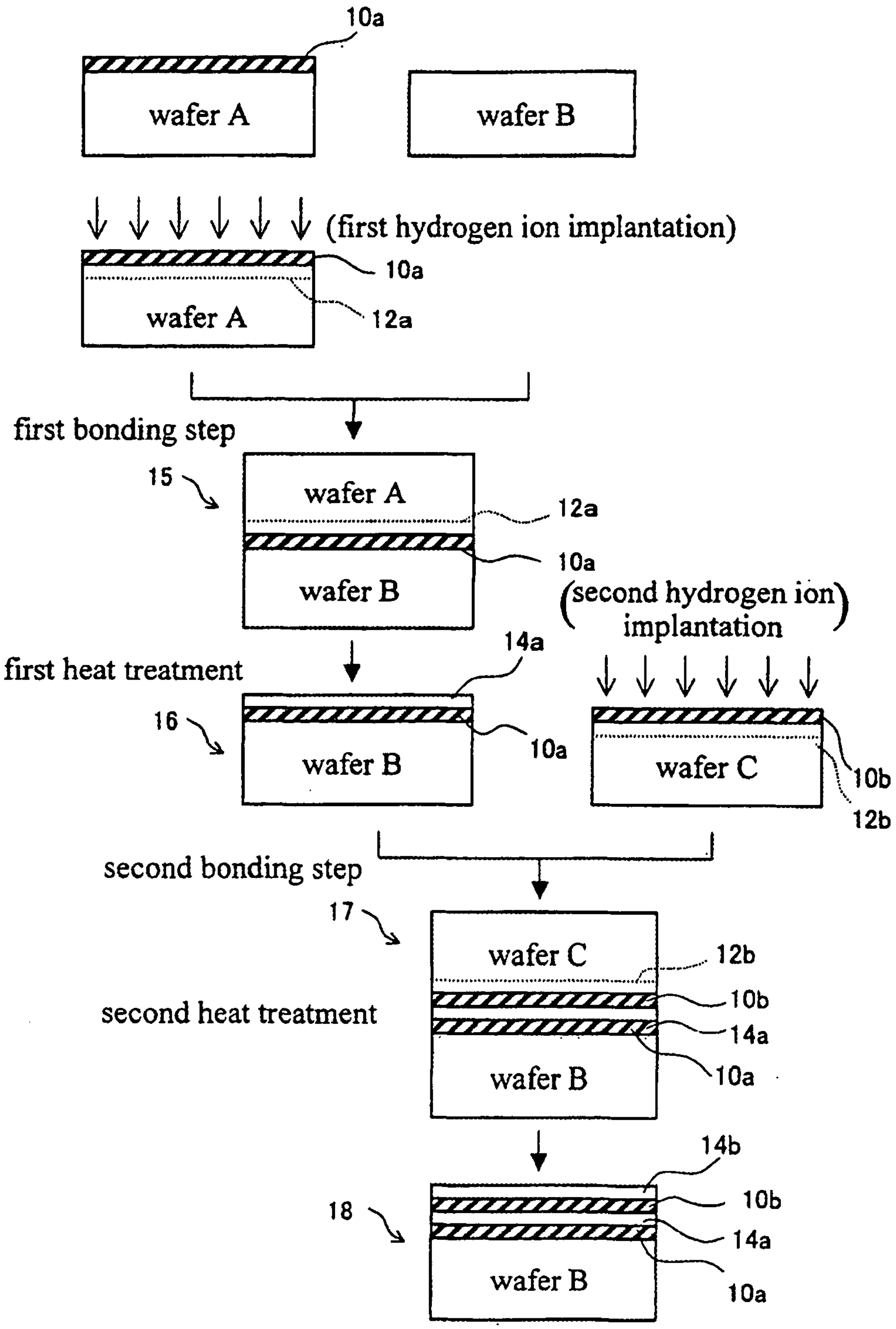

oxygen ion implantation
wafer A
wafer B
first heat treatment
wafer A
hydrogen ion implantation
wafer A
bonding step
wafer A
wafer B
second heat treatment
wafer B

FIG. 4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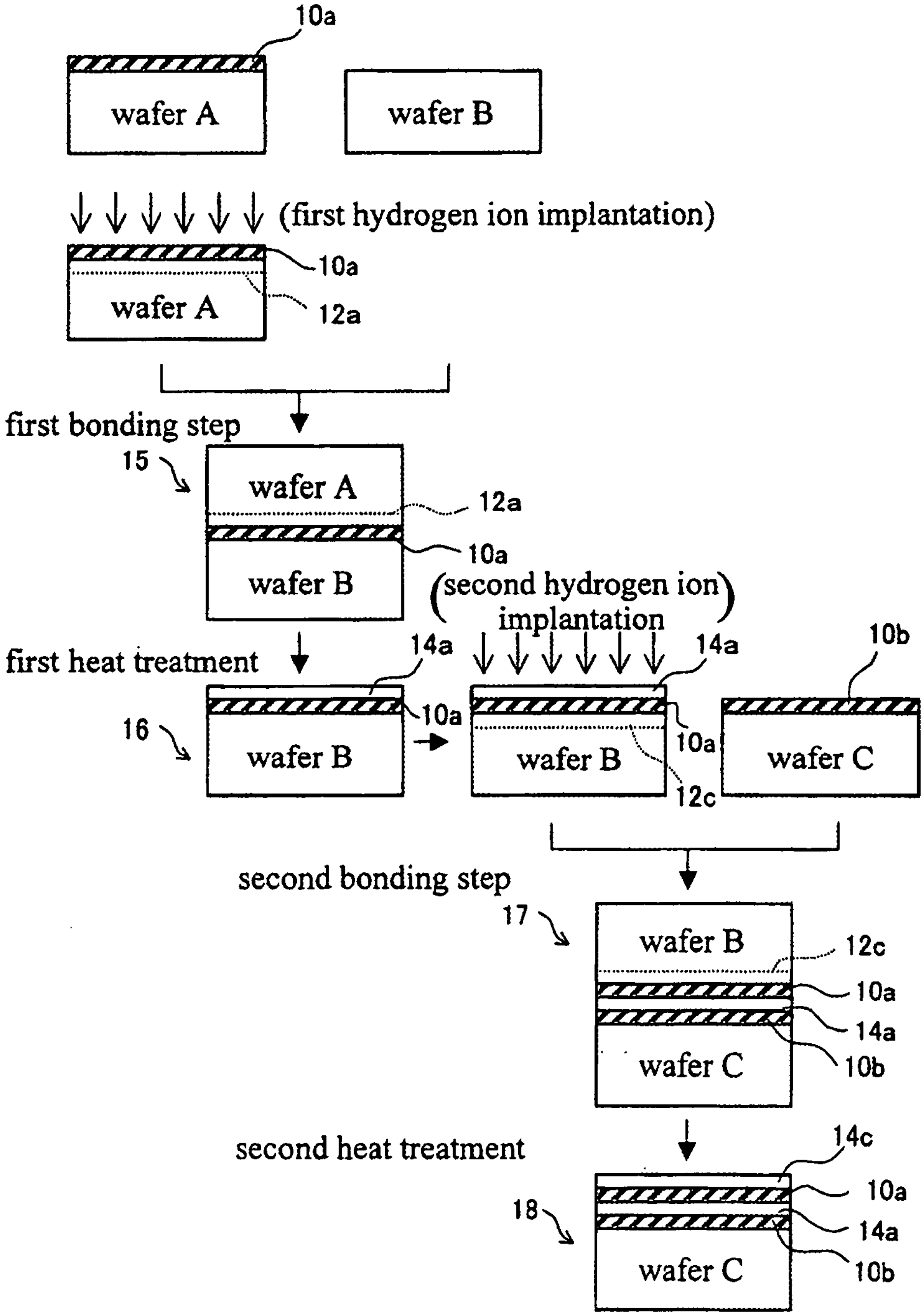
wafer A
wafer B
(first hydrogen ion implantation)
10a
wafer A
12a
first bonding step
15
wafer A
12a
10a
wafer B
(second hydrogen ion implantation)
first heat treatment
14a
16
10a
wafer B
wafer C
10b
12b
second bonding step
17
wafer C
12b
10b
second heat treatment
14a
wafer B
10a
14b
10b
18
14a
wafer B
10a

FIG. 5


10a
wafer A
wafer B
(first hydrogen ion implantation)
10a
wafer A
12a
first bonding step
15
wafer A
12a
10a
wafer B
(second hydrogen ion implantation)
first heat treatment
14a
10a
16
wafer B
14a
10a
wafer B
12c
10b
wafer C
second bonding step
17
wafer B
12c
10a
14a
wafer C
10b
second heat treatment
14c
10a
18
14a
wafer C
10b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/00331

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl^{7} H01L27/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl^{7} H01L27/12, H01L21/26-21/268, H01L21/322-21/326, H01L21/02, H01L21/70-21/74, H01L21/76-21/765, H01L21/77, G02B5/20-5/28, G02B6/12-6/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2001
Kokai Jitsuyo Shinan Koho	1971-2001	Jitsuyo Shinan Toroku Koho	1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	US, 5494846, A (NEC Corporation), 27 February, 1996 (27.02.96),	
X	Full text; Figs. 23, 24	1,2
A	Full text; Figs. 23, 24 & JP, 7-176608, A Full text; Figs. 21, 25	3-5
	US, 5953622, A (Hyundai Electronic Industries Co., Ltd.), 14 September, 1999 (14.09.99),	
X	Full text; Figs. 1 to 12	3
A	Full text; Figs. 1 to 12 & JP, 10-172918, A Full text; Figs. 1 to 11 & KR, 98038049, A	4,5
	EP, 0953853, A (SHIN-ETSU HANDOTAI COMPANY LIMITED), 03 November, 1999 (03.11.99),	
Y	Full text; Figs. 1 to 11	1,2
A	Full text; Figs. 1 to 11 & JP, 11-316154, A Full text; Figs. 1 to 11	3-5

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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INTERNATIONAL SEARCH REPORT

International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	A. Rickman, et al., "Low-Loss Planar Optical Waveguides Fabricated in SIMOX Material", IEEE PHOTONICS TECHNOLOGY LETTERS, VOL.4, NO.6,(06.92),	
Y	pp. 633-635	1,2
A	pp. 633-635	3-5
A	T. W. Ang, et al., "0.15dB/cm loss in Unibond SOI wavelength", ELECTRONICS LETTERS, Vol.35, No.12, (10.06.99), pp.977-978	1-5
A	JP, 5-299345, A (Nippon Steel Corporation), 12 November, 1993 (12.11.93), Full text; Figs. 1 to 3 (Family: none)	1-5

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